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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,153	08/04/2003	Ward D. Parkinson	ITO.0553US (P16341)	5107

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,153	PARKINSON ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Applicant's response filed on 7/5/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-25** are pending for examination.

Claim Rejections - 35 USC § 103

1. Claims **1-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ovshinsky (RE37,259), Klersy et al (5,933,365), or Czubatyj et al (5,825,046).**

The reasons for this rejection has been set forth in the last Office action dated 4/26/2005, and the applicant's remarks concerning the applicability of these references' teachings toward the claims are not found persuasive for the following stated reasons:

- Regarding **Ovshinsky (RE37259)** patent, col. 1 (lines 26-27) from this patent specifically stated that "**Ovonic EEPROM** is capable of storing **both analog and digital forms of information**" for storage (emphasis added). Thus, the pure knowledge of using phase-change material to store analog information, besides digital values, has been previously known and widely acknowledged; and therefore, one skilled in the art can use this patent disclosure to make/produce a memory **to store only data/information in the analog form (without any digital states or conversions**) by this statement's implication, if desired, and so the applicant's arguments are not convincing; Furthermore, this patent clearly teaches away the applicant's claims **2 & 7** because both these claims also specifically reciting that **information/data can be stored in either digital**

or analog form (see claim 2) and also **in at least three different resistance values (see claim 7)** which is also consistent with the disclosure of this patent's suggestion in terms of a wide range of number of states detected by changed resistances from each memory cell (i.e., gray scale or pseudo-analog);

- Regarding **Kersky (5,933,365),** col. 1 (lines 20-22) from this patent specifically stated that "**Ovonic EEPROM** is capable of **both analog and digital forms of information**" for storage (emphasis added). Thus, the pure knowledge of using phase-change material to store analog information, besides digital values, has been previously known and acknowledged; and therefore, one skilled in the art can obviously use this patent disclosure to make/produce a memory **to store only data/information in the analog form (without any digital states or conversions)**, if desired, and so the applicant's arguments are not convincing; Furthermore, this patent also particularly teaches away the applicant's claims 2 & 7 because both these claims also specifically reciting that **information/data can be stored in either digital or analog form** (see claim **2**) and **also information can be stored in at least three different resistance values** (see claim **7**) which is consistent with the disclosure of this patent in terms of a wide range of number of states detected by changed resistances from each memory cell (i.e., either gray scale or pseudo-analog forms). Particularly, col. 18 (lines 1-13) discussed

the use of a "dynamic" range of sub-ranges of resistances that can allow the creating of any multi-level analog form in terms of 2^n storage levels.

- Regarding **Czubatyj et al patent (5,825,046),** col. 1 (lines 21-23) from this patent specifically stated that "**Ovonic EEPROM** is capable of **both analog and digital forms of information**" for storage (emphasis added). Thus, the suggested knowledge of using phase-change material to store analog information, besides digital values, has been previously known and acknowledged; and therefore, one skilled in the art can obviously use this patent disclosure to make/produce a memory **to store only data/information in the analog form (without any digital states or conversions**), if desired, and so the applicant's arguments are not convincing; Furthermore, this patent also particularly teaches away the applicant's claims 2 & 7 because both these claims also specifically reciting that **information/data "can be stored in either digital or analog form"** (see claim **2**) and **also information can be stored "in at least three different resistance values"** (see claim **7**) which is consistent with the disclosure of this patent in terms of a wide range of number of states detected by changed resistances from each memory cell (i.e., either gray scale or pseudo-analog forms). Particularly, col. 18 (lines 1-13) discussed the use of a "dynamic" range of resistances that can allow the creating of a multi-level analog form in terms of 2^n storage levels.

2. The last rejections of claims **1-25** over **Gonzalez, Gilton, Lung, and Zahorik** patents have been withdrawn since these do not clearly spelled out anywhere that information/data can be stored in analog form as pointed out in the applicant's remarks.

3. Claims **1-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Van Brocklin et al (6,879,525), or Czubatyj (4,782,340).**

This newly discovered art of **Van Brocklin et al (see Fig. 3)** also teaches the use of a phase-change material with changeable resistance (element 52) and be programmed by the applied current/voltage device 70) in order to store the magnitude of information representing the data in analog form. Information read out can be detected and/or written by measured using the read-out current using the DAC (digital-to-analog converter unit 80) through read-out resistor element (74). Thus, since read out current going through the programmable resistor (52) from each cell is already in the analog form (***even though this patent does not specifically spelled out that analog is the only stored form allowed)***, it still would have been obvious to one skilled in this art that by changing the magnitude of such applied voltage or applied current (with continuous varying values/waveforms) going through the op-amp (66) and into the cell (56), any amount of analog data can be stored in terms of its continuous varying analog voltage levels and/or amplitudes instead of just pure digital levels/states as compared with other conventional non-volatile, threshold memory devices. For example, col. 2(lines 55-67) stated that the **electrical parameters** such as, i.e.,

voltage or current, going through each stored cell is continuous because it is handled by a current **continuously feedback device**. Thus, each cell is not stored in terms of states but can be used to store in multiple states or continuous varying (current) levels if desired. Furthermore, when/if any digital values/states are to be used, col. 5 (lines 32-37) sated that "any amount of states could theoretically be implemented.." thus also obviously suggest that an unlimited amount or continuous varying range of voltage levels can be stored, which also means that the whole range of analog voltage levels that a resistor can store to represent any data in any analog form/level as well, etc. Finally, Fig. 4 also shows that the stored current value, if any, of memory cell (**see predetermined value C, Figs. 3 & 4**) read out form each cell is also "**continuously varying**" with "continuously" increasing values over the programming period because the shape of its current waveform is analog changing with stair-case increasing values, and thus has no stored "**discrete**" or "**gray scale**" states, etc.

Regarding other claimed features concerning the use of sense amplifier, read/write devices or current control devices using current sensing techniques are obviously seen in Figs. **2, 3, & 6** of this patent.

Similarly, the patent of **Czubatyj (see Fig. 1)** teaches the use of a phase-change material (i.e., col.2, lines 65-68) inside a memory cell to store data by programming its **continuously varying resistance values** to represent multitude of data levels. It is noted even though this patent does not stated specifically that its memory design can be used to store only in "analog" form.

Yet, **col. 2 (lines 25-35)** specifically stated that information **can be stored in by applied signals or waveforms, or in any other analog forms, or in any other electrically detectable form**, etc., thus obviously indicate to one skilled in this art the other possibility of using applied currents or applied voltages for storing/transforming these direct values into the cell resistance values (& in only analog form) as another alternative, if desired. Detected or read-out currents, if any, thus can be interpreted as analog or converted into digital states if desired. However, the stored data must be in analog forms (as it is in the forms of continuously current or analog values only).

Regarding other claimed features concerning the use of sense amplifier, read/write devices or current control devices using current sensing techniques are obviously seen in Figs. **4, 6, 8, 10, & 32** of this patent.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen